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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/879,806	06/12/2001	Alex Wayne Hietala	2867-127	3717

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EXAMINER	
PERILLA, JASON M	

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 11/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/879,806	HIETALA, ALEX WAYNE	
	Examiner	Art Unit	
	Jason M Perilla	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3,5-8,13,20 and 21* is/are rejected.

7)☒ Claim(s) *1,2,4,9-12,14-19,22 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 June 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/01 5/02 6/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-23 are pending in the instant application.

Information Disclosure Statement

2. The information disclosure statements (IDS) submitted on August 29, 2001, May 7, 2002, and June 3, 2002 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the first and second mutually exclusive control signals of claim 12 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement

Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claims 1-23 are objected to because of the following informalities:

Regarding claim 1, in line 8, the phrase "said I analog modulation signals" is lacking antecedent basis and should be replaced by --said sequence of I analog modulation signals--, in line 13, the phrase "said Q analog modulation signals" is lacking antecedent basis and should be replaced by --said sequence of Q analog modulation signals--, in line 15, the phrase "transforming said I and Q digital output signals" should be replaced by –transforming said sequences of I and Q digital output signals--, and, in line 18, the phrase "said variable divisor" should be replaced by –said variable fractional divisor--.

Regarding claim 2, the instances of the phrase "said I analog signals" in the claim should be replaced by –said sequence of I analog modulation signals—, and the instances of the phrase "said Q analog signals" in the claim should be replaced by –said sequence of Q analog modulation signals--. Further, in line 2, "a predetermined function of maximum absolute value of positive peak values" should be replaced by –a predetermined function of a maximum absolute value of positive peak values, and a corresponding amendment should be made in line 6.

Regarding claim 3, the instances of "said I analog signals" should be replaced with --said sequence of I analog modulation signals--, and the instances of "said Q analog signals" should be replaced by –said sequence of Q analog modulation signals--.

Regarding claim 6, the instances of "said I digital output values" should be replaced with --said I digital output signals--, and the instances of "said Q digital output values" should be replaced by –said Q digital output signals--.

Regarding claim 7, in line 9, "said variable divisor" should be replaced by –said variable fractional divisor--.

Regarding claim 11, in line 2, "said analog signals" should be replaced by –said analog modulation signals--.

Regarding claim 13, in line 9, "receiving first and second output digital signals" should be replaced by –receiving said first and second output digital signals--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 3, 5, and 6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 3, the use of the term "substantially" can not be definitively used to describe or limit an amount of equality with respect to a real number. One skilled in

the art is not able to determine a definitive limitation provided by the term "substantially" as used in the claim. While the use of the term "substantially" may be considered to be definite when it takes a meaning such as "mostly", in this case, a definite interpretation may not be made.

Regarding claim 5 recites the limitation "said modulation signals" in line 1. There is insufficient antecedent basis for this limitation in the claim. Further, the lack of clear antecedent basis makes the claim indefinite because more than one type of modulation signals are already defined in the parent claims.

Regarding claim 6, the claim is rejected as being based upon a rejected parent claim.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 7, 8, 13, 20, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Collins (US 5337024; IDS 8/29/01, reference "V") in view of Cooper (US 6002356).

Regarding claim 7, Collins discloses by figure 2 a radio transmitter having a fractional-N synthesizer (F-N synthesizer) (abstract) comprising a loop divider (30) having a variable fractional divisor (30), a method for generating digital modulation signals (via ADC; 42) in response to input analog modulation signals (M) and modifying

said variable fractional divisor in accordance with said digital modulation signals (col. 2, lines 25-45; col. 3, line 50-col. 4, line 9). Although Collins discloses generating digital modulation signals in response to input analog modulation signals, Collins does not explicitly disclose (a) comparing said analog modulation signals at a plurality of successive time intervals with at least one predetermined threshold value to derive a sequence of digital values, and (b) decoding said sequence of digital values to generate a corresponding sequence of digital modulation signals. However, Cooper teaches an analog to digital converter meeting the limitations of (a) by figure 1. In figure 1, Cooper discloses an analog to digital converter wherein said analog modulation signals ($+V_{IN}$) are compared (one of 15, 22, 21... 20) with at least one predetermined threshold (negative inputs to comparators off voltage tree) to derive a sequence of digital values (outputs of comparators) (col. 1, lines 18-57). It is inherent that the each time an analog input is applied to the analog to digital converter, it is considered as a successive time interval. Further, Cooper discloses the limitations of (b) being decoding (via fig 1, ref. 17) the sequence of digital values (outputs of comparators) to generate a corresponding sequence of digital modulation signals (fig. 1, "PARALLEL BINARY OUTPUTS; col. 1, line 59-col. 2, line 9). Cooper teaches that the disclosed analog to digital converter is extremely fast and can convert an analog signal into a digital format with high resolution (col. 2, lines 5-10). Therefore, it would have been obvious to one having ordinary skill in the art to utilize the analog to digital converter of Cooper meeting the limitations of (a) and (b) in place of the analog to digital converter of Collins because it is an exemplary analog to digital converter being fast and capable of a high resolution conversion.

Regarding claim 8, Collins in view of Cooper disclose the limitations of claim 7 as applied above. Collins in view of Cooper do not explicitly disclose that the at least one predetermined threshold value (Cooper; fig. 2, negative input to top comparator) comprises at least one value equal to a predetermined function of a peak value of said analog modulation signals. However, the value of $V_{REF\ HIGH}$ in figure 2 of Cooper is dependent upon the peak value of the input analog modulation signal (positive inputs to comparators). For the utility of proper comparing of the input analog modulation signal by the analog to digital converter, the value of $V_{REF\ HIGH}$ would be appropriately chosen as a function of (equivalent to or slightly higher than) the peak value of the input analog modulation signal as understood by one having ordinary skill in the art. Thereby, the value of the at least one predetermined threshold would be effectively chosen according to a predetermined peak of the input analog modulation signal. In the analog to digital converter of Collins, it is required by the design of the circuit of figure 2, that the value of $V_{REF\ HIGH}$ must be chosen according to the peak value of the input analog modulation signal. Otherwise, the analog to digital converter would not have utility because it could not make proper comparisons throughout the full range of the input analog modulation signal voltage (col. 3, line 58-col. 4, line 11). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to select the at least one predetermined threshold value as a predetermined function of the peak value of the input analog modulation signal for the utility of the proper operation of the analog to digital converter of Collins.

Regarding claim 13, Collins discloses by figure 2 a signal converter comprising an input circuit (42; col. 4, lines 3-5) for receiving analog modulation signals, and a divider circuit (30; col. 3, lines 50-57) having a variable fractional divisor determined by digital modulation signals (M) output from the input circuit. Collins does not disclose (a) that the input circuit comprises at least one comparator for comparing at least one of said analog modulation signals with at least one threshold signal level to produce a first output digital signal when said at least one analog modulation signal bears a first relationship to said at least one threshold signal level and to produce a second output digital signal when said at least one analog modulation signal bears a second relationship to said at least one threshold signal level or (b) a decoder for receiving first and second output digital signals from said at least one comparator and outputting digital modulation signals corresponding to said analog modulation signals. However, Cooper teaches by figure 1 an analog to digital converter or analog input circuit meeting the limitations of (a). In figure 1, Cooper teaches an analog to digital converter wherein said input analog modulation signals ($+V_{IN}$) are compared by at least one comparator (one of 15, 22, 21... 20) with at least one predetermined threshold (negative inputs to comparators off voltage tree) to derive a digital output (outputs of comparators) (col. 1, lines 18-57). The comparators each produce either a first output digital signal (a digital "1") or a second output digital signal (a digital "0") (col. 1, lines 44-58). Further, Cooper teaches a decoder (fig. 1, ref. 17) for receiving the first and second digital output signals from the comparator and outputting digital modulation signals corresponding to said analog modulation signals (fig. 1, "PARALLEL BINARY OUTPUTS; col. 1, line 59-col. 2,

line 9). Cooper teaches that the disclosed analog to digital converter is extremely fast and can convert an analog signal into a digital format with high resolution (col. 2, lines 5-10). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize the analog to digital converter of Cooper meeting the limitations of (a) and (b) in place of the analog input circuit of Collins because it is an exemplary analog to digital converter being fast and capable of a high resolution conversion.

Regarding claim 20, Collins in view of Cooper disclose the limitations of claim 13 above. Further, the loop divider of Collins (fig. 2, ref. 30) is a loop divider in a fractional-N (F-N) synthesizer (abstract).

Regarding claim 21, Collins in view of Cooper disclose the limitations of claim 20 as applied above. Further, Collins discloses a switch (fig. 2, ref, 44; col. 4, lines 5-10) for applying digital modulation signals from said decoder to said divider.

Allowable Subject Matter

9. Indication of allowable subject matter is made regarding claims 1-2, and 4.

10. The following is a statement of reasons for the indication of allowable subject matter:

Indication of allowable subject matter is made regarding claims 1-4 because the prior art of record does not disclose or make obvious all of the limitations of claim 1. Specifically, the prior art of record does not show the input of both I and Q modulated analog signals as input to a fractional divider decoding input.

11. Claims 9-12, 14-19, 22 and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following prior art of record not relied upon above is cited to further show the state of the art with respect to fractional-N synthesizers.

U.S. Pat. No. 6047029 to Eriksson et al.

U.S. Pat. No. 6011815 to Eriksson et al.

U.S. Pat. No. 6380809 to Camp Jr.

U.S. Pat. No. 6044124 to Monahan et al.

U.S. Pat. No. 6002273 to Humphreys.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M Perilla whose telephone number is (571) 272-3055. The examiner can normally be reached on M-F 8-5 EST.

13. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Chin can be reached on (571) 272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason M. Perilla
October 25, 2004

jmp

CHIEH M. FAN
PRIMARY EXAMINER